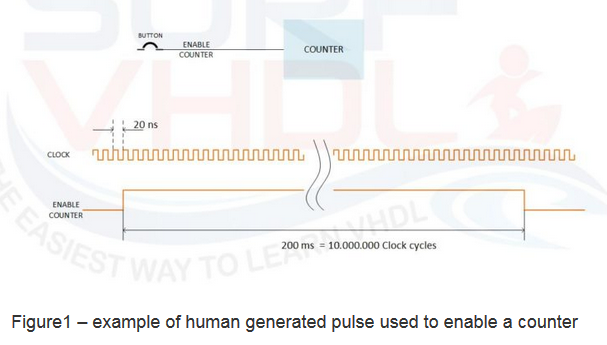
In digital synchronous design sometimes we need to detect the transition ‘0’->’1′ or ‘1’->’0’ of a signal.

As a simple example, suppose you have a counter with enable input port connected to an external push button. You need to count +1 every time you push the button.



Let the counter clock to be for example 50 MHz. The clock period is 20 ns. Even if you are very very fast in pushing the button it will be difficult to generate a pulse of 20 ns in order to enable the counter for only one clock cycle.

For example, if you push the button even for few millisecond, let say for instance 200 ms, your counter will be enabled for 200 ms/20 ns = 10.000.000 of clock cycle!

As you can see we need another solution than trying to push the button very very fast!

The solution is to implement something that is able to detect the transition of our input signal: an edge detector, no matter how long your control signal remains high, you are detecting the transition from ‘0’ to ‘1’.

In this case, we have the opposite problem: the control signal shall remain high at least 2 clock cycle (remember Nyquist theorem? ) to be sure to sample the signal correctly.

Using the architecture in Figure2, we can generate a pulse of one clock, no matter how long is the input control signal, so every time we push the button we will count +1.